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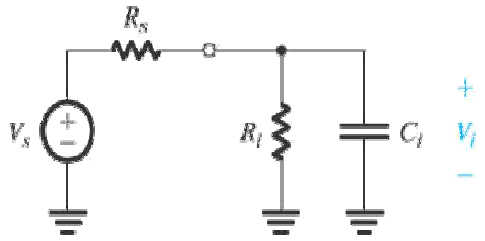
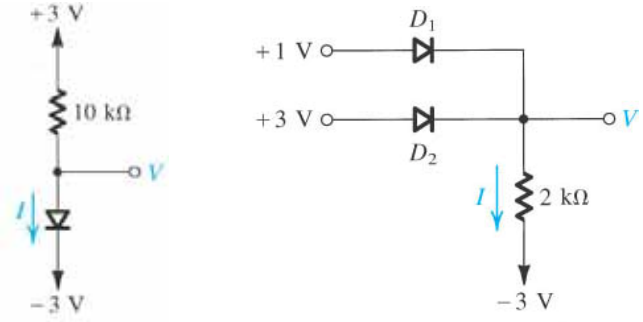
1. The following figure shows a signal source connected to the input of an amplifier. Here R_s is the source resistance, and R_i and C_i are the input resistance and input capacitance, respectively, of the amplifier. Derive an expression for $V_i(s)/V_s(s)$. Is this circuit a high-pass, low-pass, or band-pass filter? Find the 3-dB frequency for the case R_s = 20 kΩ, R_i = 80 kΩ, and C_i = 5 pF.



2. Assuming that the diodes in the circuits of the following figures are ideal, find the values of the labeled voltage and currents.



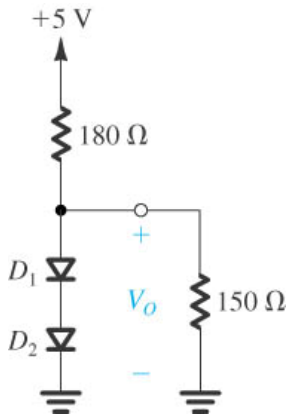
(a) (b)

3. A particular design of a voltage regulator is shown below. Diode D_1 and D_2 are 10 mA units; that is, each has a voltage drop of 0.7 V at a current of 10 mA. Each has n = 1.

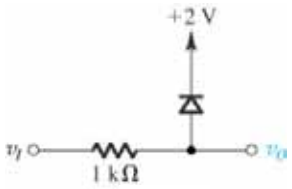
   (a) Find V_O with no load.

   (b) What is the regular output voltage V_O with the 150 Ω load connected?

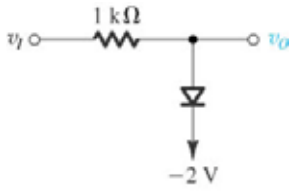
   (c) With the load connected, to what value can the 5 V supply be lowered while maintaining the loaded output voltage within 0.1 V of its nominal value?



4. Sketch the transfer characteristic v_O versus v_I for the limiter circuits shown in the following figures, assuming that the diodes are modeled with the piecewise-linear model with $V_{D0} = 0.65$ V and $r_D = 20\ \Omega$.

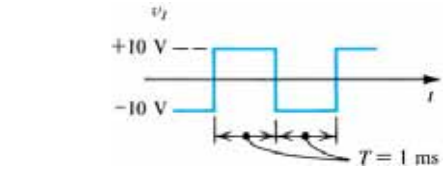


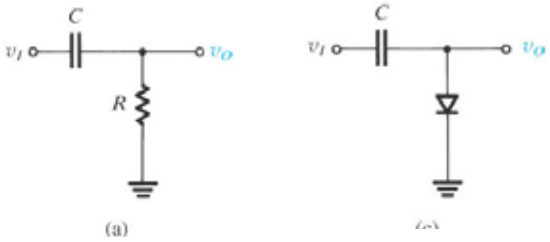
(a)



(b

5. For the circuits in the following figures, each utilizing an ideal diode, sketch the output for the input shown. Label the most positive and most negative output levels. Assume $CR >> T$. (15%)





(a) (b)

6. An n-channel device has $k_n' = 50\ \mu A/V^2$, $V_t = 0.8$ V, and $W/L = 20$. The device is to operate as a switch for small v_{DS}, utilizing a control voltage v_{GS} in the range 0 V to 5 V. Find the switch closure resistance, r_{DS}, and closure voltage, V_{DS}, obtained when $v_{GS} = 5$ V and $i_D = 1$ mA.

7. Consider a CMOS process for which $L_{min} = 0.8\ \mu m$, $\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m, $t_{ox} = 15$ nm, $u_n = 550\ cm^2/V.s$, and $V_t = 0.7$ V.

   (a) Find C_{ox} and k_n'.

   (b) For an NMOS transistor with $W/L = 16\ \mu m/0.8\ \mu m$, calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\ \mu A$.

   (c) For the device in (b), find the value of V_{OV} and V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}.

8. An NMOS transistor, fabricated with $W = 100\ \mu m$ and $L = 5\ \mu m$ in a technology for which $k_n' = 50\ \mu A/V^2$ and $V_t = 1$V, is to be operated at very low values of v_{DS} as linear resistor. For v_{GS} varying from 1.1 V to 11 V, what range of resistor values can be obtained? What is the available range if

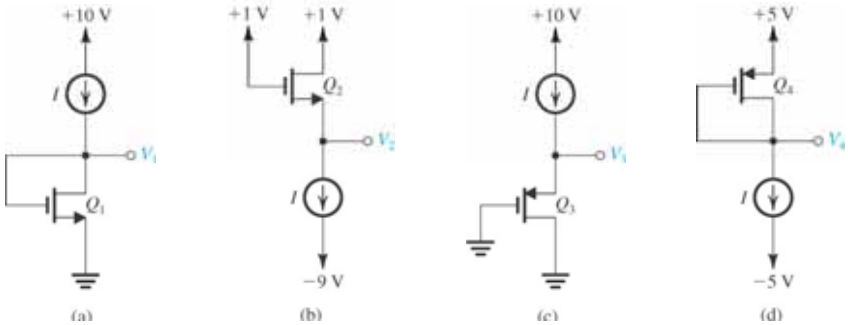
   (a) the device width is halved?

   (b) the device length is halved?

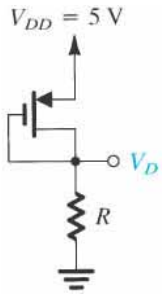
   (c) both the width and length are halved?

9. An NMOS transistor is fabricated in a 0.8 μm process having $k_n' = 130\ \mu A/V^2$ and $V_A' = 20\ V/\mu m$ of channel length. If $L = 1.6\ \mu m$ and $W = 16\ \mu m$, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5 V and $V_{DS} = 2$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 1 V, what is the corresponding change in I_D?

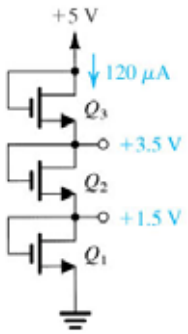
10. All the transistors in the circuits shown below have the same values of $|V_t|$, k', W/L, and λ. Moreover, λ is negligibly small. All operate in saturation at $I_D = I$ and $|V_{GS}| = |V_{DS}| = 3$ V. Find the voltages V_1, V_2, V_3, and V_4. If $|V_t| = 1$ V and $I = 2$ mA, how large a resistor can be inserted in series with each drain connection while maintaining saturation? What is the largest resistor that can be placed in series with each gate? If the current source I requires at least 2 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring saturated-mode operation of each transistor at $I_D = I$? In the latter limiting situation, what do V_1, V_2, V_3, and V_4 become?



11. The PMOS transistor in the circuit below has $V_t = -0.7$ V, $u_pC_{ox} = 60\ \mu A/V^2$, $L = 0.8\ \mu m$, and λ= 0. find the values required for W and R in order to establish a drain current of 115 μA and a voltage V_D of 3.5 V.



12. The NMOS transistors in the circuit below have $V_t = 1$ V, $u_nC_{ox} = 120\ \mu A/V^2$, λ= 0, and $L_1 = L_2 = L_3 = 1\ \mu m$. Find the required values of gate width for each of Q_1, Q_2, and Q_3 to obtain the voltage and current values indicated.

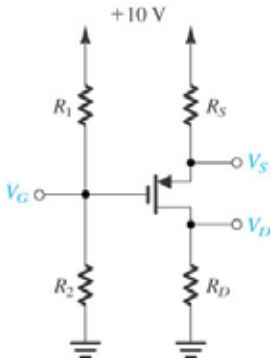


13. Design the circuit below so that the transistor operates in saturation with V_D biased 1 V from the edge of the triode region, with I_D = 1 mA and V_D = 3 V, for each of the following two devices (use a 10 μA current in the voltage divider):

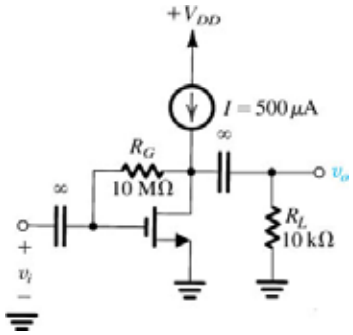
    (a) $|V_t|$ = 1 V and $k_p'W/L$ = 0.5 mA/V^2

    (b)$|V_t|$ = 2 V and $k_p'W$/L = 1.25 mA/V^2

    For each case specify the values of V_G, V_S, R_1, R_2, R_S, and R_D.



14. In the circuit below, the NMOS transistor has $|V_t|$ = 0.9 V and V_A = 50 V and operates with V_D = 2 V. What is the voltage gain v_o/v_i? what do V_D and the gain become for I increased to 1 mA?



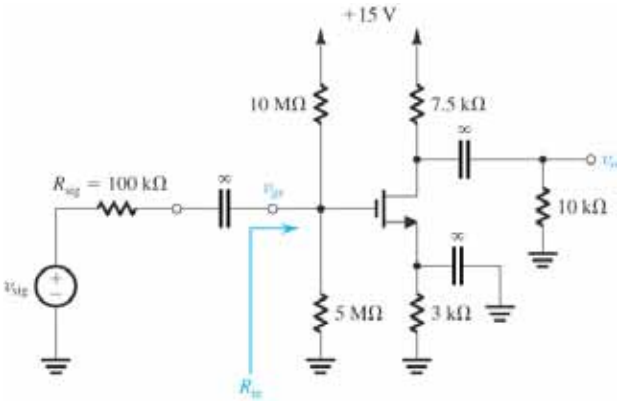
15. The figure below shows a discrete-circuit CS amplifier employing the classical biasing scheme. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

(a) If the transistor has $V_t = 1$ V, and $k_n'W/L = 2$ mA/V^2, verify that the bias circuit establishes $V_{GS} = 2$ V, $I_D = 1$ mA, and $V_D = +7.5$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.

(b) Find g_m and r_o if $V_A = 100$ V.

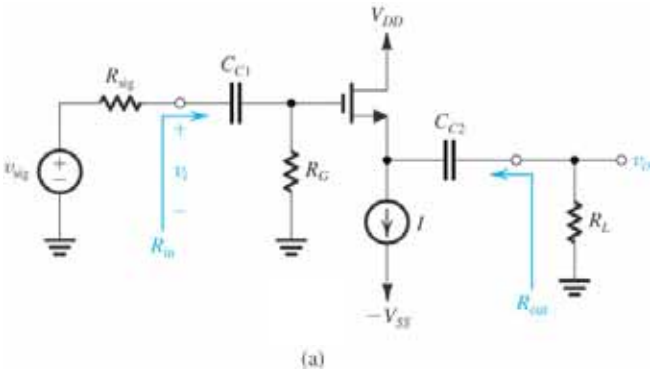
(c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies.

(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}



16. A common-gate amplifier using an *n*-channel enhancement MOS transistor for which $g_m = 5$ mA/V has a 5 kΩ drain resistance (R_D) and a 2 kΩ load resistance (R_L). The amplifier is driven by a voltage source having a 200Ω resistance. What is the input resistance of the amplifier? What is the overall voltage gain G_v? If the circuit allows a bias-current increase by a factor of 4 while maintaining linear operation, what do the input resistance and voltage gain become?

17. The source follower below uses a MOSFET biased to have $g_m = 5$ mA/V and $r_o = 20$ kΩ. Find the open-circuit voltage gain A_{vo} and the output resistance. What will the gain become when a 1 kΩ load resistance (R_L) is connected?



18. The MOSFET in the circuit below has $V_t = 1$ V, $k_n'W/L = 0.8$ mA/V^2, and $V_A = 40$ V.

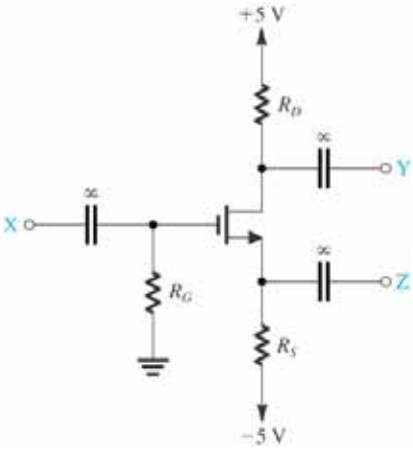
(a) Find the values of R_S, R_D, and R_G so that $I_D = 0.1$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±1 V is possible, and the input resistance at the gate is 10 MΩ.

(b) Find the values of g_m and r_o at the bias point.

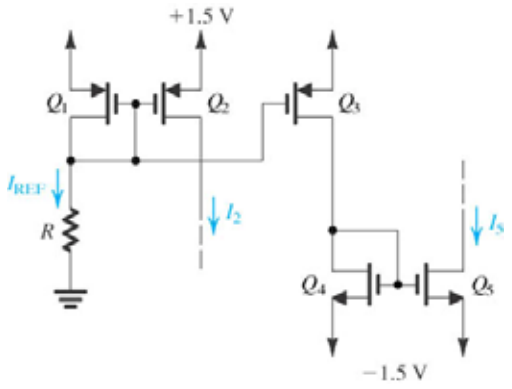
(c) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 40 kΩ, find the voltage gain form signal source to load.

(d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?

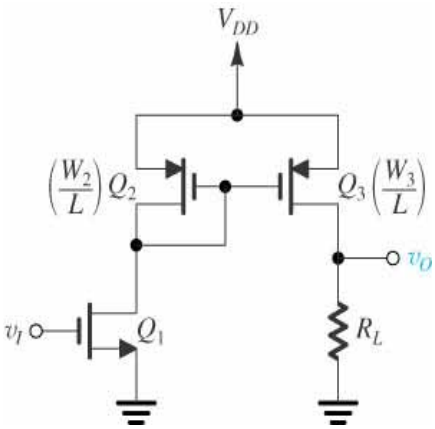
(e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 10 μA and having a resistance of 100 kΩ, find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o.



19. The current-steering circuit below is fabricated in a CMOS technology for which u_nC_{ox} = 200 μA/V^2, u_pC_{ox} = 80 μA/V^2, V_{tn} = 0.6 V, V_{tp} = -0.6 V, V_{An}' = 10 V/μm, and $|V_{Ap}'|$ = 12 V/μm. If all devices have L = 0.8 μm, design the circuit so that I_{REF} = 20 μA, I_2 = 100 μA, $I_3 = I_4$ = 20 μA, and I_5 = 50 μA. Use the minimum possible device widths while achieving proper operation of the current source Q_2 for voltages at its drain as high at +1.3 V and proper operation of the current sink Q_5 with voltages at its drain as low as -1.3 V. Specify the widths of all devices and the values of R. Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5.

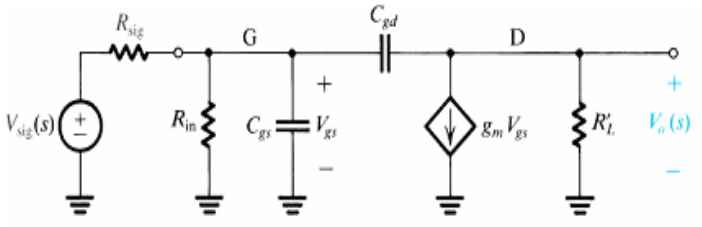


20. A signal-current amplifier is illustrated below. Here Q_1 is a common-source amplifier fed with $v_I = V_{GS} + v_i$, where V_{GS} is the gate-to-source dc bias voltage of Q_1 and v_i is a small signal to be amplified. Find the signal component of the output voltage v_O and hence the small-signal voltage gain v_o/v_i.

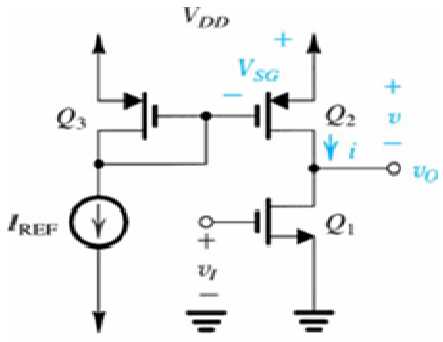


21. Find the midband gain A_M and the upper 3-dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_{sig} = 100 kΩ. The amplifier has R_G = 4.7 MΩ, R_D = R_L = 15 kΩ, g_m = 1mA/V, r_o = 150 kΩ, C_{gs} = 1 pF, and C_{gd} = 0.4 pF.

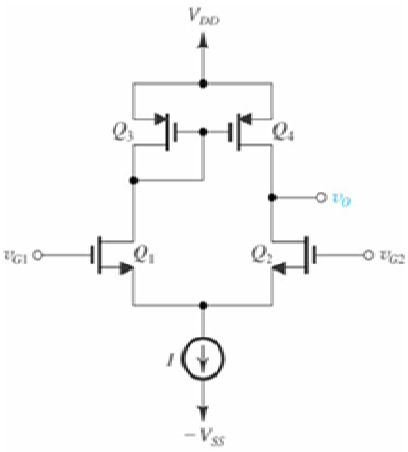
22. The following figure shows the high-frequency equivalent circuit of a common-source FET amplifier. The amplifier is fed with a signal generator V_{sig} having a resistance R_{sig}. Resistance R_{in} is due to the biasing network. Resistance R_L' is the parallel equivalent of the load resistance R_L, the drain bias resistance R_D, and the FET output resistance r_o. Capacitors C_{gs} and C_{gd} are the FET internal capacitances. For R_{sig} = 100kΩ, R_{in} = 420kΩ, C_{gs} = C_{gd} = 1pF, g_m = 4mA/V, and R_L' = 3.33kΩ, find the midband voltage gain, $A_M = V_o/V_{sig}$, the upper 3-dB frequency, f_H, and the gain-bandwidth product in megahertz. Moreover, find the value of R_L' that will result in f_H = 180kHz. Find the new values of the midband gain and of the gain-bandwidth product.



23. A CMOS common-source amplifier of the type shown in the following figure has W/L = 7.2μm/0.36μm for all transistors, $\mu_n C_{ox}$ = 387 μA/V^2, $\mu_p C_{ox}$ = 86 μA/V^2, I_{REF} = 100 μA, V_{An}' = 5V/μm, and $|V_{Ap}'|$ = 6V/μm. For Q_1, C_{gs} = 20fF, C_{gd} = 5fF, C_L = 25fF, and R_{sig} = 10kΩ. Assume that C_L includes all the capacitances introduced by Q_2 at the output node. Find f_H using both the Miller equivalence and the open-circuit time constants. Also, determine the exact values of f_{P1}, f_{P2}, and f_Z and hence provide another estimate for f_H.



24. Consider an active-loaded MOS differential amplifier of the type shown in the following figure. Assume that for all transistors, W/L = 7.2μm/0.36μm, C_{gs} = 20fF, C_{gd} = 5fF, and C_{db} = 5fF. Also, let $\mu_n C_{ox}$ = 387 μA/V^2, $\mu_p C_{ox}$ = 86 μA/V^2, V'_{An} = 5 V/μm, $|V'_{Ap}|$ = 6 V/μm. The bias current I = 0.2mA, and the bias current source has an output resistance R_{SS} = 25kΩ and an output capacitance C_{SS} = 0.2pF. In addition to the capacitances introduced by the transistors at the output node, there is a capacitance C_x of 25fF. It is required to determine the low-frequency values of A_d, A_{cm}, and CMRR. It is also required to find the poles and zero of A_d and the dominant pole of CMRR.



25. An amplifier has the voltage transfer function

$$T(s) = \frac{10s}{(1+s/10^2)(1+s/10^5)}$$

Find the poles and zeros and sketch the magnitude of the gain versus frequency. Find approximate values for the gain at ω=10, 10^3, and 10^6 rad/s. Find the Bode plot for the phase of the transfer function of the amplifier .

26. The noninverting op amp configuration shown in the figure provides a direct implementation of the feedback loop.

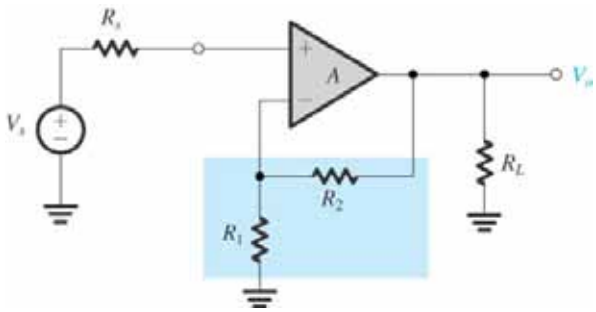
(a) Assume that the op amp has infinite input resistance and zero output resistance. Find an expression for the feedback factor β.

(b) If the open-loop voltage gain A=10^4, find R_2/R_1 to obtain a closed-loop voltage gain A_f of 10

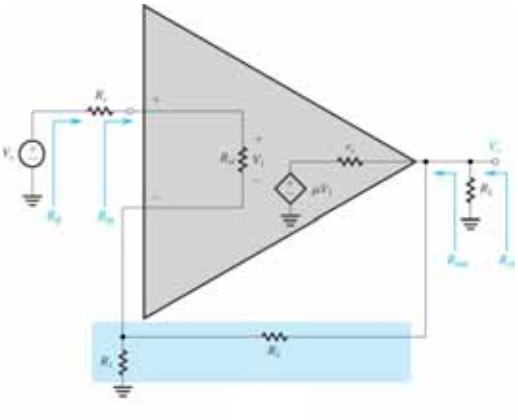
(c) What is the amount of feedback in decibels?

(d) If V_s = 1V, find V_o, V_f, and V_i.

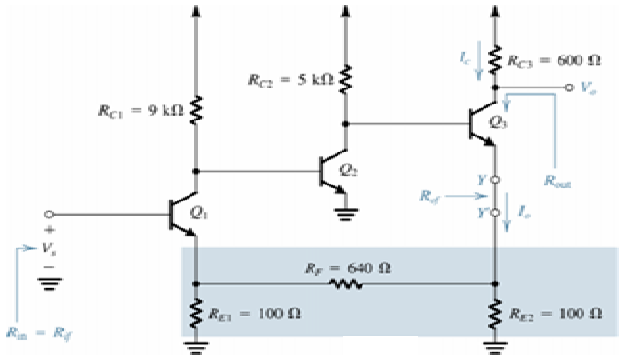
(e) If A decreases by 20%, what is the corresponding decrease in A_f?



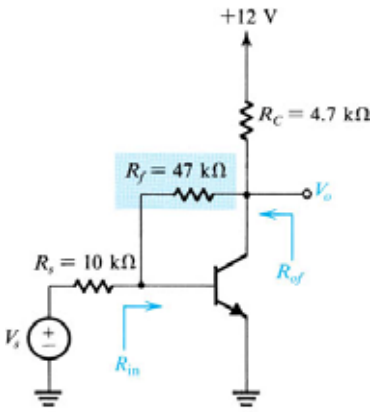
27. The figure below shows an op amp connected in the noninverting configuration. The op amp has an open-loop gain μ, a differential input resistance R_{id}, and an output resistance r_o. Here we wish to use the feedback method to analyze the circuit taking both R_{id} and r_o into account. Find expressions for A, β, the closed-loop gain V_o/V_s, the input resistance R_{in} (see the figure), and the output resistance R_{out}. Also find numerical values, given $\mu = 10^4$, $R_{id} = 100\text{k}\Omega$, $r_o = 1\text{k}\Omega$, $R_L = 2\text{k}\Omega$, $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{M}\Omega$, and $R_s = 10\text{k}\Omega$.



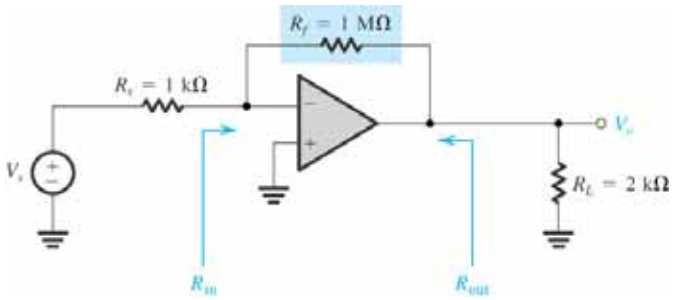
28. Because negative feedback extends the amplifier bandwidth, it is commonly used in the design of broadband amplifiers. One such amplifier is the MC1553. Part of the circuit of the MC1553 is shown in the following figure. The circuit shown (called a feedback triple) is composed of three gain stages with series-series feedback provided by the network composed of R_{E1}, R_F, and R_{E2}. Assume that the bias circuit, which is not shown, causes $I_{C1} = 0.6\text{mA}$, $I_{C2} = 1\text{mA}$, and $I_{C3} = 4\text{mA}$. Using these values and assuming $h_{fe} = 100$ and $r_o = \infty$, find the open-loop gain A, the feedback factor β, the closed loop gain $A_f = I_o/V_s$, the voltage gain V_o/V_s, the input resistance $R_{in} = R_{if}$, and the output resistance R_{of} (between nodes Y and Y', as indicated). Now if r_o of Q_3 is 25kΩ, estimate an approximate value of the output resistance R_{out}.



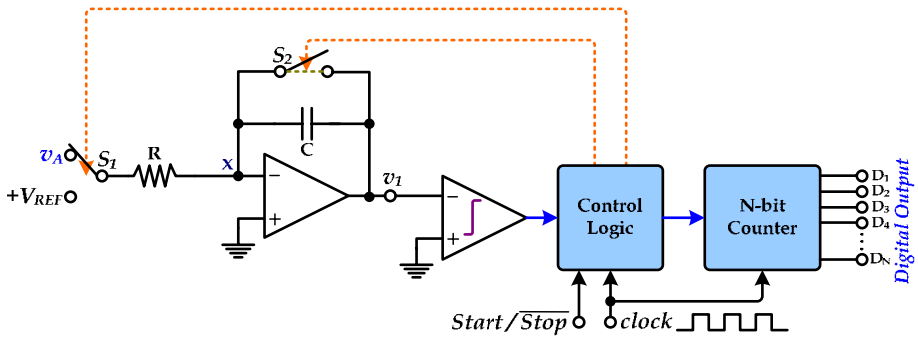
29. We want to analyze the circuit of the figure below to determine the small-signal voltage gain V_o/V_s, the input resistance R_{in}, and the output resistance $R_{out} = R_{of}$. The transistor has $\beta = 100$.



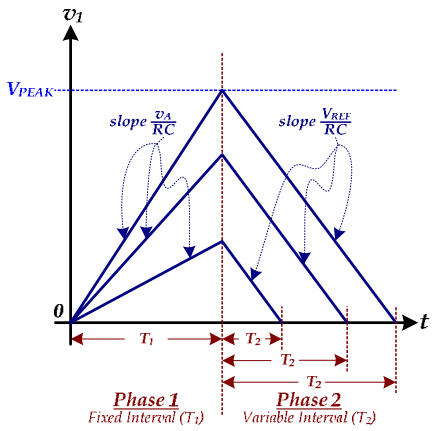
30. Use the feedback method to find the voltage gain V_o/V_s, the input resistance R_{in}, and the output resistance R_{out} of the inverting op amp configuration of the figure below. Let the op amp have open-loop gain $\mu = 10^4$, $R_{id} = 100\text{k}\Omega$, and $r_o = 1\text{k}\Omega$.



31. A 12-bit dual-slope ADC of the type illustrate in the figure below utilizes a 1-MHz clock and has $V_{REF} = 10\text{V}$. Its analog input voltage is in the range 0 to -10V. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N. What is the time required to convert an input voltage equal to the full-scale value? If the peak voltage reached at the output of the integrator is 10V, what is the integrator time constant? If through aging, R increase by 2% and C decreases by 1%, what does V_{PEAK} become? Does the conversion accuracy change?



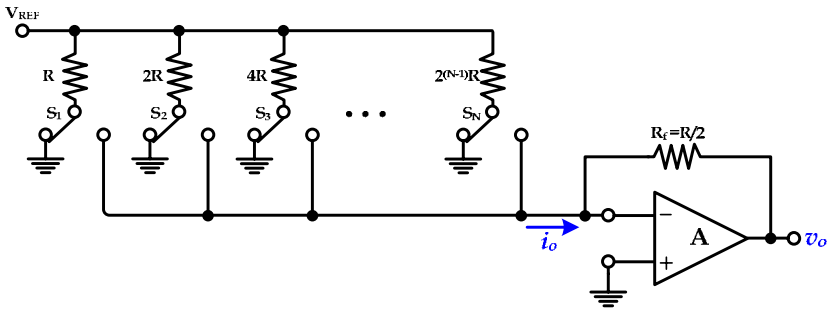
(a)



(b)

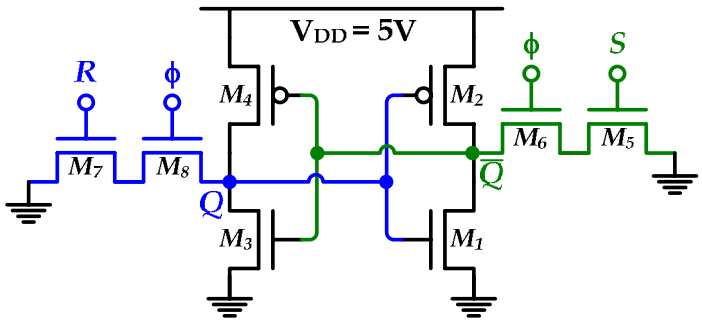
The dual-slope A/D conversion method. Note that v_A is assumed to be negative.

32. Consider the DAC circuit of the figure below for the cases $N = 2$, 4, and 8. What is the tolerance, expressed as $\pm x\%$, to which the resistors should be selected to limit the resulting output error to the equivalent of $\pm 1/2$ LSB%.



An N-bit D/A converter using a binary-weighted resistive ladder network.

33. For a Flip-flop of the type shown in the figure below, determine the minimum width required of the set (S) and reset (R) pulse. Let M_1~M_4 be minimum-size devices for which W/L = 2μm/1μm and all other devices have W/L = 4μm/1μm. V_{DD} = 5V, $|V_T|$ = 1V, $k_n' = 2.5k_p' = 100$ μA/V^2, and the total capacitance at each of nodes Q and $\overline{Q}$ is 30fF.



CMOS implementation of a clocked SR flip-flop.

34. In a particular 1G-bit memory of the dynamic type (called DRAM) under development by Samsung, using a 0.16̃ μm, 2-V technology, the cell array occupies about 50% of the area of the 21 mm × 31 mm chip. Estimate the cell area. If two cells form a square, estimate the cell dimensions.

35. For a particular DRAM design, the cell capacitance Cs = 50pF, V_{DD} = 5V, and V_T = 1.4V. Each cell represents a capacitive load on the bit line of 2-fF. The sense amplifier and other circuitry attached to the bit line has a 20-fF capacitance. What is the maximum number of cells that can be attached to a bit line while ensuring a minimum bit-line signal of 0.1V? How many bits of row addressing can be used? If the sense-amplifier gain is increased by a factor of 5, how many word-line address bits can be accommodated?

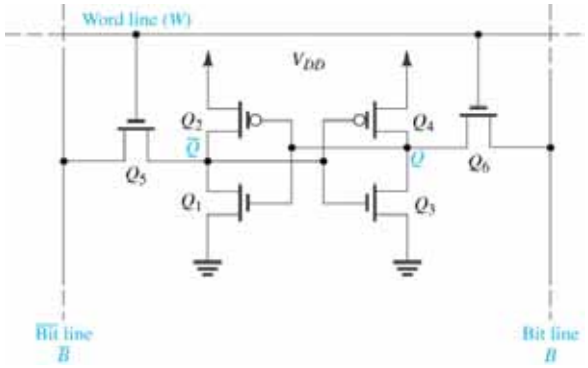
36. Consider the write operation of the SRAM cell of the figure below. Specifically, refer to relevant parts of the circuit, as depicted in the figure. Let the process technology be characterized by $\mu_n/\mu_p = 2.5$, $\mu_p C_{ox} = 20$ μA/V^2, $|V_{t0}| = 0.8$V, $2\phi_f = 0.6$V, $\gamma = 0.5$V$^{0.5}$, $V_{DD} = 5$V. Also let each of the two inverters be matched and $(W/L)_1 = (W/L)_3 = n$, where n denoted the W/L ratio of a minimum-size device.

(a) Using the circuit in Fig. (a), find the minimum required (W/L) of Q_5 (in terms of n) so that node $\overline{Q}$ can be pulled to $V_{DD}/2$, that is, at $v_{\overline{Q}} = 2.5$V, $I_5 = I_1$.

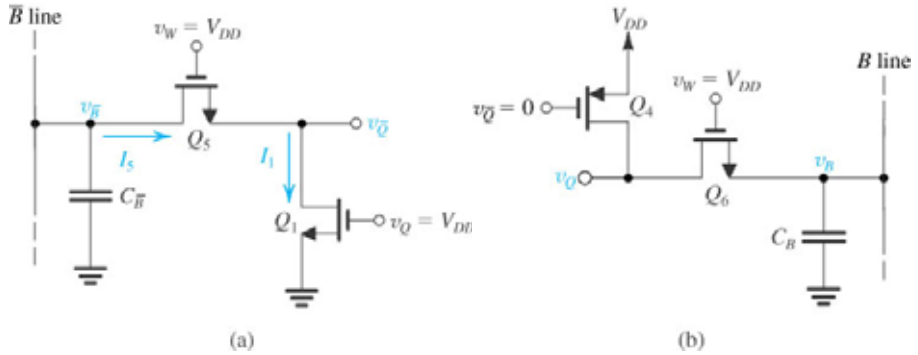
(b) Using the circuit of Fig. (b), find the minimum required (W/L) of Q_6 (in terms of n) so that node Q can be pulled down to $V_{DD}/2$, that is, at $v_Q = 2.5$V, $I_6 = I_4$.

(c) Since Q_5 and Q_6 are designed to have equal W/L ratios, which of the two values found in (a) and (b) would you choose for a conservative design?

(d) For the value found in (c) and for $n = 2$, and $\mu_n C_{ox} = 50$μA/V^2, determine the time for v_Q to reach $V_{DD}/2$. Let $C_Q = 50$fF.

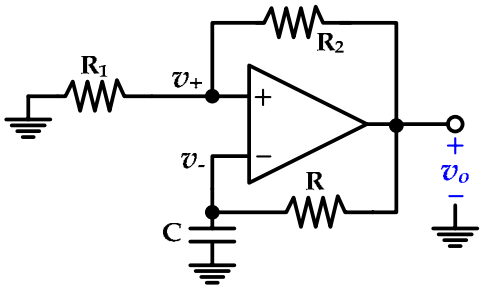


CMOS SRAM Cell

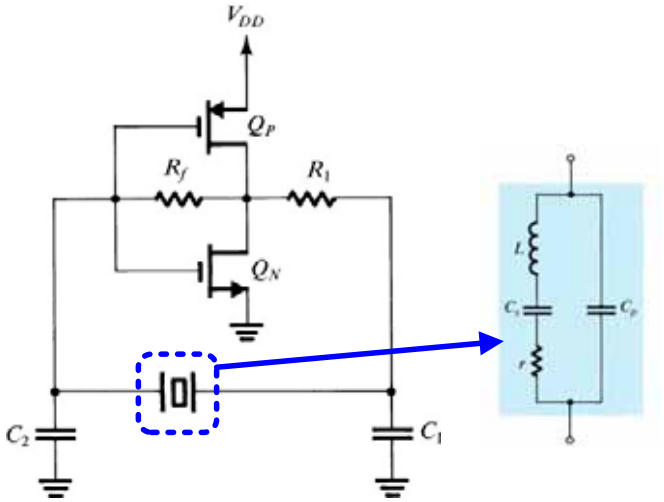


Write Operation

37. Find the frequency of oscillation of the circuit shown in the figure below for the case R_1 = 10KΩ, R_2 = 16KΩ, C = 10nF, and R = 62KΩ.

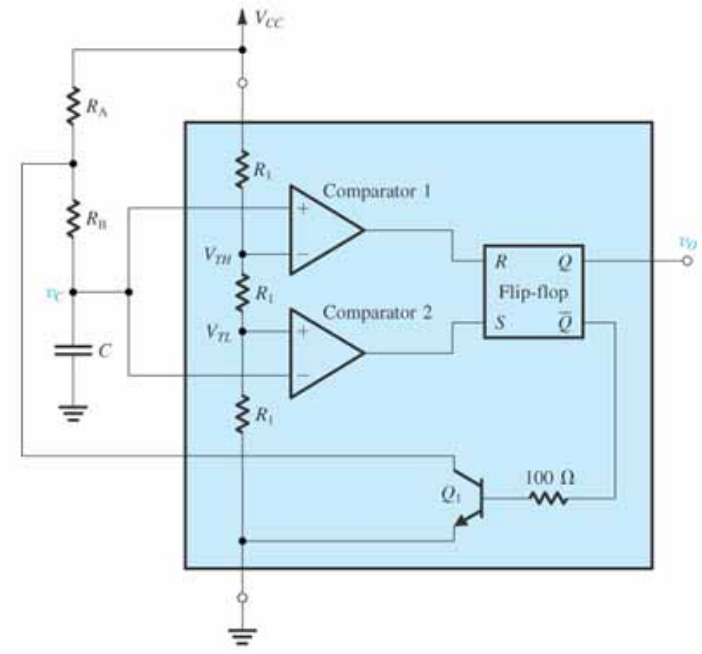


38. Consider the Pierce crystal oscillator of the figure below. The quartz crystal is specified to have L = 0.52H, C_s = 0.012pF, C_p = 4pF, and r = 120Ω. Let C_1 be variable in the range 1pF to 10pF, and Let C_2 be fixed at 10pF. Find the range over which the oscillation frequency can be tuned.



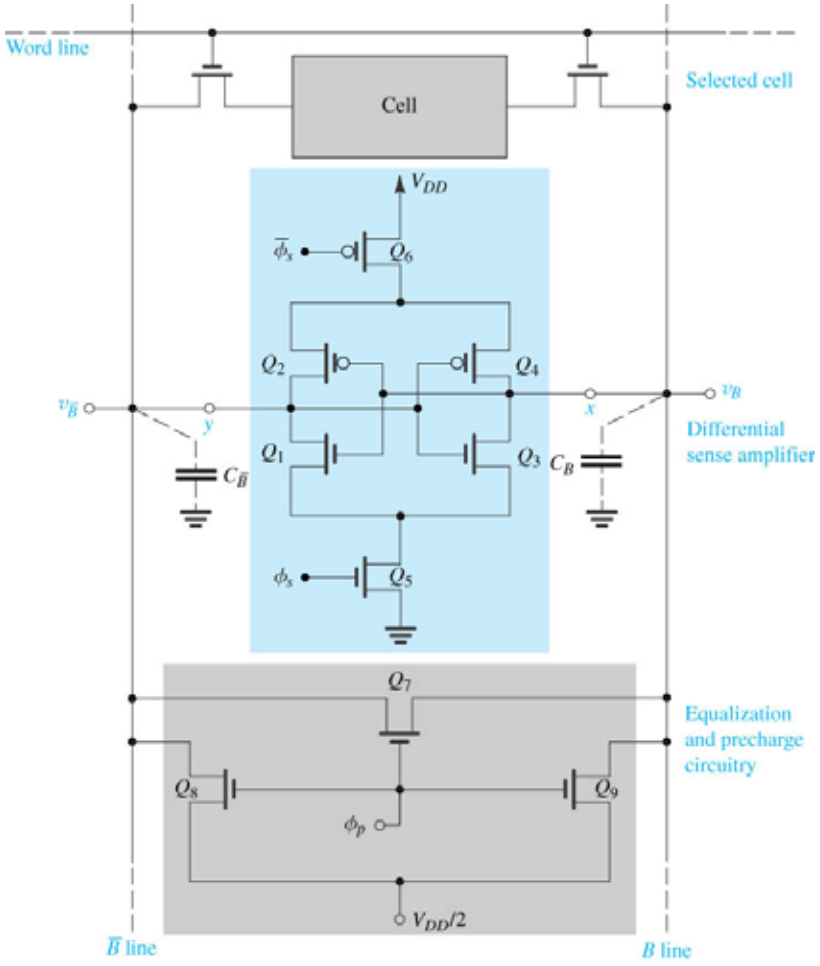
Pierce crystal oscillator

39. Using a 680pF capacitor, design the astable circuit of the figure below to obtain a square wave with a 50kHz frequency and a 75% duty cycle. Specify the values of R_A and R_B.



An astable multivibrator implemented by the 555 timer.

40. Consider the operation of the differential sense amplifier of the figure below following the rise of the sense control signal ϕ_s. Assume that a balanced differential signal of 0.1V is established between the bit lines each of which has a 1-pF capacitance. For V_{DD} = 3V, what is the value of G_m of each of the inverters in the amplifier required to cause the outputs to reach 0.1 V_{DD} and 0.9 V_{DD} (from initial values of $0.5V_{DD}$ + (0.1/2) and $0.5V_{DD}$ – (0.1/2) volts, respectively) in 2 ns? If for the matched inverters, $|V_t|$ = 0.8V and $k_n' = 3k_p' = 75$ μA/V^2, what are the device widths required? If the input signal is 0.2V, what does the amplifier response time become?



A differential sense amplifier